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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,917	11/21/2003	Toshihide Tsubata	1035-482	7569

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,917	TSUBATA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,19-21,25,26,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,19-21,25,26,33 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 September 2007 has been entered.

Claims 1 and 3-9, 19-21, 25-26 and 33-34 are pending. Claims 2, 10-18, 22-24, 27-32 and 35 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 24 May 2007 with respect to claims 1 and 3-11, 13-14, 16-17 and 18-34 have been fully considered but they are not persuasive.

On page 11, first paragraph of the response, the applicant argues that Matsuo may illustrate a gap, but that the gap must be taken in combination with the conductive nature of the black mask. Further the applicant argues that the insulating property not being essential and the applicant having different embodiments with different features and advantages does not militate against patentability. The examiner respectfully

disagrees. The fact that the applicant has disclosed of both having a conductive light shielding film and a insulating light shielding film without disclosing the specific advantages of having such in their specification proves that these features are not essential to their invention. That being said, the combination of the references made by the examiner would teach of both having an insulating black matrix and a conductive black matrix. Therefore, it would have been an obvious design choice to one of ordinary skill in the art at the time the invention was made to use either a conductive or insulating black matrix. The fact that Matsuo discloses of a conductive black matrix being used in his invention does not mean that his teaching of providing a gap is insignificant. Matsuo's teaching can still be applied to the teachings of AAPA, and the conductive or insulating nature of the black matrix after the combination would be merely a design choice to someone of ordinary skill in the art.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 4, 6, 8, 19-21, 25-26 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13) in view of Matsuo (JP 07-128685).

Regarding claim 1, AAPA discloses a display device substrate (Figure 13, item 110), comprising:

one or more pixel electrodes each of which is provided on each intersection of a signal line and a scanning line that are provided on an insulating substrate (Figures 12 and 13 show that pixel electrode 103' is located at the intersection of scanning line 104 and a signal line 102, and are provided on substrate 110, which it explained to be insulating on page 5, lines 16-20.); and

an interlayer insulating film stacked between the signal line and the pixel electrode (Figure 13 shows interlayer insulating film layer 115 between the signal line 102 and the pixel electrode 103'.),

wherein the signal line is covered by a light shielding film having an insulating property that is provided on the signal line (Figure 13 shows that light shielding film 108

covers signal line 102, and is explained to having an insulating property on page 6, lines 4-9.);

wherein the interlayer insulating film is provided on the light shielding film (Figure 13 shows that layer 115 is on the layer 108.); and

wherein the pixel electrode is provided on the interlayer insulating film (Figure 13 shows that pixel electrodes 103 and 103' are provided on the layer 115.).

AAPA fails to teach that in view of a vertical direction with respect to a surface of the insulating substrate, the signal line is provided on an area on which the pixel electrode is not provided, and a gap is provided between the signal line and the pixel electrode, and wherein in view of a vertical direction with respect to the surface of the insulating substrate, a surface of the signal line and the gap provided between the signal line and the pixel electrode are covered by the light shielding film.

Matsuo discloses a display device substrate (Drawing 2, substrate 9) where in view of a vertical direction with respect to a surface of the insulating substrate, the signal line is provided on an area on which the pixel electrode is not provided, and a gap is provided between the signal line and the pixel electrode (Drawings 1 and 2 shows that there is a gap between the signal lines 2 and the pixel electrode 3.), and wherein in view of a vertical direction with respect to the surface of the insulating substrate, a surface of the signal line and the gap provided between the signal line and the pixel electrode are covered by a light shielding film (Drawing 1 and 2 show that the black matrix 8 covers a surface of the signal line 2 and the gap.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to provide a gap between the signal line and the pixel electrode as taught by Matsuo with the substrate structure taught by AAPA in order to reduce capacitive coupling of a pixel electrode and a source that causes unevenness and crosstalk of the vertical direction.

Also, previously it was claimed that the black layer was both conductive and insulating, which clearly indicates that having one or the other is merely a design choice and that the invention would work both ways. Thus the light shielding film being insulating is not essential to the invention. Since the rejection is using AAPA and Matsuo in combination, then the combination actually teaches both ideas and making the black matrix conductive or insulating does not matter. Therefore, it would have been an obvious design choice to one of ordinary skill in the art at the time the invention was made to use either a conductive or insulating black matrix.

Regarding claim 4, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with surface of the insulating substrate, respect to the a gap between the pixel electrodes which are adjacent to each other with the signal line there between is covered by the light shielding film (Drawings 1 and 2 show that the gap between the pixel electrode 3 is covered by the light shielding film 8.).

Regarding claim 6, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also disclose a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.); and

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and

(ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 8, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Drawings 1 and 2 show that a contact hole electrically connects active portion 10 to pixel electrode 3, as explained in paragraphs [0003] and [0011].); and

a light shielding film provided so as to cover surfaces of the active element, the signal line, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 19, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also disclose wherein the gap is set to be within a range of from not less than 1μm to not more than 20μm (It would be inherent that the gap between the pixel electrode 3 and signal line 2 taught by Mutsumi would be within a range of from not less than 1μm to not more than 20μm.).

Regarding claim 20, AAPA and Matsuo disclose a liquid crystal display device, comprising the display device substrate as set forth in claim 1 (Paragraph [0001] of Matsuo).

Regarding claim 21, please refer to the rejection of claim 1, and furthermore it would be inherent that there are plural pixel electrodes.

AAPA and Matsuo fail to teach of a size of the gap being set to provide a desired ΔΔβ value which is interrelated with display unevenness, however, since when a gap is introduced between the pixel electrodes and signal lines display unevenness is reduced, it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the gap to a desired value to provide the best display characteristics possible.

Regarding claim 25, AAPA and Matsuo disclose a display device substrate as set forth in claim 22.

AAPA also disclose a display device substrate wherein the light shielding film covers a signal line associated with a first pixel electrode and is overlapped by a second pixel electrode (Figure 13 shows pixel electrode 103 and pixel electrode 103' respectively), the first pixel electrode being directly driven by the signal line and the second pixel electrode not being directly driven by the signal line (Pixel electrode 103 is connected to the drain and therefore is directly driven and since 103' is not connected it is not directly driven.).

Matsuo also disclose of a display device wherein an overlap of the second pixel electrode and the light shielding film having a width y (Drawing 2 shows that there is an overlap between the pixel electrode 3 and the black matrix 8 that has some width.).

AAPA and Matsuo fail to teach wherein y is not less than 0.6 μm and not more than 5 μm, however, it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the overlap to a desired width in order to provide the best display characteristics possible.

Regarding claim 26, AAPA and Matsuo disclose a display device substrate as set forth in claim 21, wherein the desired ΔΔβ value is not more than 0.08 (It would be inherent that the value would be less than 0.08 in order to provide a optimal display.).

Regarding claim 33, please refer to the rejection of claims 21-22, and furthermore AAPA also disclose a display device substrate wherein the light shielding film having an insulating property covers a signal line associated with a first pixel

electrode and is overlapped by a second pixel electrode (Figure 13 shows pixel electrode 103 and pixel electrode 103' respectively), the first pixel electrode being directly driven by the signal line and the second pixel electrode not being directly driven by the signal line (Pixel electrode 103 is connected to the drain and therefore is directly driven and since 103' is not connected it is not directly driven.).

Matsuo also disclose of a display device wherein an overlap of the second pixel electrode and the light shielding film having a width y (Drawing 2 shows that there is an overlap between the pixel electrode 3 and the black matrix 8 that has some width.) and whereby a gap of width x is provided between the signal line and the pixel electrode (Drawing 2 shows that there is a gap between the pixel electrode and the signal line that has some width.).

AAPA and Matsuo fail to teach wherein y is not less than 0.6 μm and not more than 5 μm and wherein x is in the rang of no less than 1 μm and not more than 20 μm, however, it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the overlap and gap to desired widths in order to provide the best display characteristics possible.

Regarding claim 34, AAPA and Matsuo disclose a display device substrate as set forth in claim 33.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each respective intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the

active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

wherein the light shielding film is provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.).

6. Claims 3, 5, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13) in view of Matsuo (JP 07-128685) and further in view of Zhang et al. (US 6,396,470).

Regarding claims 3, 5, 7 and 9, AAPA and Matsuo disclose the display device substrate as set forth in claims 2, 4, 6, 8, 10, 13 and 16.

AAPA and Matsuo fail to teach wherein the light shielding film is made of resin having an insulating property.

Zhang et al. disclose of a light shielding film made of resin having an insulating property (Column 12, lines 54-63 explain that the light shielding film shown in Figure 8 is an insulating black resin.).

Therefore it would have been obvious to "one of ordinary skill" ion the art at the time the invention was made that the light shielding film taught by the combination of AAPA and Matsuo be made of an insulating resin as taught by Zhang et al. in order to allow the light shielding film to be forming in a desired area without using a resist mask.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

5 October 2007